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ReS_2-Based Field-Effect Transistors and Photodetectors

Enze Zhang, Yibo Jin, Xiang Yuan, Weiyi Wang, Cheng Zhang, Lei Tang, Shanshan Liu, Peng Zhou, Weida Hu,* and Faxian Xiu**

Atomically thin 2D layered transition metal dichalcogenides (TMDs) have been extensively studied in recent years because of their appealing electrical and optical properties. Here, the fabrication of ReS_2 field-effect transistors is reported via the encapsulation of ReS_2 nanosheets in a high-κ Al_2O_3 dielectric environment. Low-temperature transport measurements allow to observe a direct metal-to-insulator transition originating from strong electron–electron interactions. Remarkably, the photodetectors based on ReS_2 exhibit gate-tunable photoresponsivity up to 16.14 A W^{-1} and external quantum efficiency reaching 3168%, showing a competitive device performance to those reported in graphene, $MoSe_2$, GaS, and GaSe-based photodetectors. This study unambiguously distinguishes ReS_2 as a new candidate for future applications in electronics and optoelectronics.

1. Introduction

Two-dimensional materials like graphene and MoS_2 have been widely studied because of their intriguing physical properties and promising applications in optoelectronic and spintronic devices.[1–4] Due to its mechanical flexibility and high carrier mobility, graphene has been incorporated into transparent devices for electrodes and high-speed photodetectors as channel material.[5–7] Importantly, because of its small intrinsic spin–orbit coupling and vanishing hyperfine interaction, extensive research has been devoted to graphene spintronics.[8,9] However, despite these substantial efforts, owing to its zero band gap the graphene-channeled devices typically possess a low on/off ratio that significantly impedes its applications.

MoS_2, as an exemplary member of 2D layered transition metal dichalcogenides (TMDs), exhibits a transition from an indirect band gap (1.2 eV) to a direct band gap (1.8 eV) in monolayer, similar to those observed in other TMDs such as $MoSe_2$, WS_2, and WSe_2.[10–12] MoS_2 field-effect transistors (FETs)[13] show a high mobility of 200 $cm^2\ V^{-1}\ s^{-1}$ with an on/off current ratio of approximately 10^8, which can be readily applicable to Flash memory,[14–17] high-frequency,[18,19] valleytronic and spintronic devices.[20–22] However, the exploration of other members in the TMDs family is still at the early stage, and new findings should be anticipated and enlightening.[23,24]

Among the TMDs family, special attention has been paid to ReS_2 because its bulk material behaves electronically and vibrationally as decoupled monolayers arising from the lack of interlayer registry and weak interlayer coupling.[25] Consequently, ReS_2 maintains a direct bandgap of 1.5 eV from bulk to monolayer.[25,26] In contrast with what has been discovered in MoS_2 and other 2D-TMDs, the unique band structure of ReS_2, irrespective to its thickness, offers exciting opportunities for achieving high-efficiency photodetectors. Although ReS_2 has been tested as a candidate material for field-effect transistors (FETs),[27] there remains an intense interest in improving the device performance and exploring low-temperature transport properties. Here, we demonstrate the fabrication of top-gate FET devices and show an on/off current ratio exceeding 10^6 at room temperature. As the measurement temperature is reduced, a metal-to-insulator transition is observed in few-layer ReS_2 devices by modulating the electric field, indicating strong electron–electron interactions. Furthermore, the ReS_2-based photodetectors provide a gate-tunable photoresponsivity up to 16.14 A W^{-1} and a high EQE of 3168%.

2. Results and Discussion

2.1. Material Synthesis and Characterization

Few-layer ReS_2 nanosheets were synthesized on SiO_2/Si substrates in a chemical vapor deposition (CVD) furnace using ReO_3 and sulfur as the source materials (see the Experimental Section). **Figure 1**a shows a typical atomic structure of ReS_2

E. Zhang, Y. Jin, X. Yuan, W. Wang, C. Zhang, L. Tang, S. Liu, Prof. F. Xiu
State Key Laboratory of Surface Physics and Department of Physics
Fudan University
Shanghai 200433, China
E-mail: faxian@fudan.edu.cn
E. Zhang, Y. Jin, X. Yuan, W. Wang, C. Zhang, L. Tang, S. Liu, Prof. F. Xiu
Collaborative Innovation Center of Advanced Microstructures
Fudan University
Shanghai 200433, China
Prof. P. Zhou
State Key Laboratory of ASIC and System
Department of Microelectronics
Fudan University
Shanghai 200433, China
E-mail: pengzhou@fudan.edu.cn
Prof. W. Hu
National Laboratory for Infrared Physics
Shanghai Institute of Technical Physics
Chinese Academy of Sciences
Shanghai 200083, China
E-mail: wdhu@mail.sitp.ac.cn

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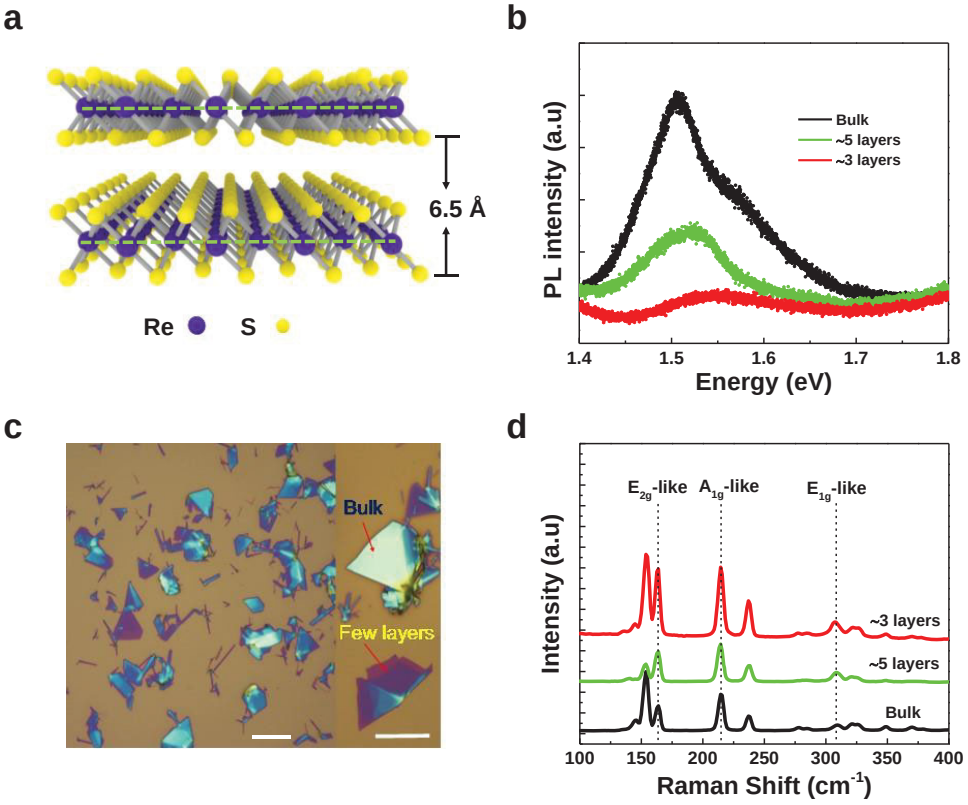

Figure 1. a) Atomic structure of ReS_2. The layer to layer distance is ≈6.5 Å. b) Room temperature PL spectra of ReS_2 with different thickness. c) Optical microscopic images of bulk and few-layer ReS_2 grown by CVD on SiO_2/Si substrate. Scale bars, 5 μm. d) Raman spectra of ReS_2.

that crystallizes in a distorted 1 T structure with clustering of Re_4 units forming a 1D chain inside each monolayer (dash line).[25,26,28] Figure 1b illustrates the photoluminescence spectra taken from three layers of ReS_2 to the bulk, where the band gap experiences negligible change from 1.54 to 1.50 eV, consistent with former studies.[25,27] Figure 1c displays the optical images of as-grown ReS_2 nanosheets. Different thicknesses can be verified though the optical contrast and precisely determined by atomic force microscopy (AFM). As expected, Raman spectroscopy shows no dependence on thickness due to the decoupling of lattice vibrations between adjacent layers (Figure 1d, also see Figure S6 in the Supporting Information).[25]

2.2. Top-Gate FET Based on Few-Layer ReS_2

Top-gate FET devices were fabricated by performing the standard e-beam lithography (EBL) and metal deposition process (see the Experimental Section). **Figure 2**a shows the schematic device structure. A 30 nm thick Al_2O_3 layer was deposited by atomic layer deposition (ALD) and the resultant Al_2O_3 serves as the top-gate dielectric material. The corresponding scanning electron microscopy (SEM) picture of the device is displayed in Figure 2c. The Fermi level of the encapsulated ReS_2 channel can be effectively tuned by changing the top-gate voltage (V_{TG}) or the back-gate voltage (V_{BG}) applied on the degenerately doped silicon substrate. To study the gate modulation of the ReS_2 nanosheets, source-drain current–voltage (I_{DS}–V_{DS}) curves at different V_{TG} were measured (Figure 2b): I_{DS} varies linearly with V_{DS}, indicating well-developed contacts between the electrodes and the ReS_2 channel. The transfer curves of the device (I_{DS}–V_{TG}) can be obtained by sweeping V_{TG} while keeping the back gate grounded. As illustrated in Figure 2d, a maximal on/off ratio more than 10^6 is acquired when V_D reaches 500 mV (I_{DS}–V_{BG}, inset of Figure 2d). Meanwhile, a subthreshold swing of 750 mV per decade is extracted, which is comparable to the reported top-gate MoS_2 FET devices.[13] Also, the calculated field-effect mobility of the device is about 1 $cm^2\ V^{-1}\ s^{-1}$ using the equation $\mu = (dI_{DS}/dV_{TG})[L/(WC_iV_{DS})]$, where L and W are the channel length and width, respectively. C_i is the capacitance per unit area between the top gate and the ReS_2 channel.

2.3. Temperature-Dependent Transport Properties of the Four-Terminal Few-Layer ReS_2 FET

Temperature-dependent transport properties were investigated using back-gated four-terminal devices, as shown in **Figure 3**b (inset). For this type of device, the measured four-probe conductance is defined as $G = I_{DS}/(V_1 - V_2)$, where I_{DS} is the source drain current and $V_1 - V_2$ is the measured voltage drop between the middle two voltage probes. Figure 3a shows double sweeps of I_{DS}–V_{DS} characteristics for the temperature range of 2–300 K at a constant V_{BG} of 40 V. Negligible hysteresis is observed and nonlinear behavior starts to disappear for the temperature above 200 K, excluding the possible influence of the contact

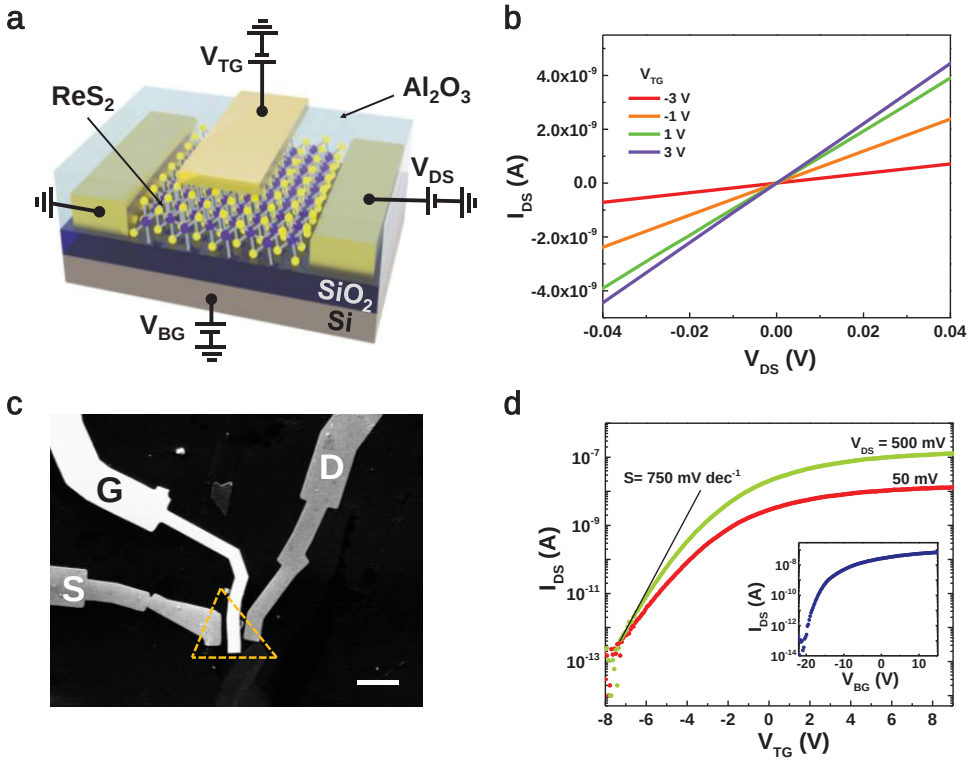

Figure 2. a) Schematic structure of ReS_2 top-gate FET. b) Output characteristics (I_{DS}–V_{DS}) of the device under different top-gate voltages. c) SEM image of the fabricated top-gate FET based on few-layer ReS_2. Scale bar, 5 μm. d) Room temperature transfer curves (I_{DS}–V_{TG}) of the device, which has an on/off current ratio of 10^6 at V_{DS} = 500 mV. Inset, I_{DS}–V_{BG} of the device obtained at V_{DS} = 100 mV.

resistance or Schottky barrier on the mobility extraction.[29] The dependence of the channel conductance G on V_{BG} at different temperatures is revealed in Figure 3b. When V_{BG} is larger than 15 V, a metallic state associated with the metal-to-insulator transition is evident due to the increase of Fermi level.[30] Also, the temperature-dependent field-effect mobility of the device, calculated by using the field-effect mobility formula, reaches its maximum value at 120 K (Figure 3c). Below this critical temperature, the mobility decreases owing to scattering from the charged impurities. Similar behavior has been observed from MOS_2 back-gate devices.[29] On the other hand, an increase in temperature has also led to the strong decrease of the mobility, which can be attributed to the electron–phonon scattering that dominates at high temperatures. The temperature dependence follows the relation $\mu \propto T^{-\gamma}$ and the temperature damping factor γ depends on electron–phonon coupling in the sample. By fitting the curve, $\gamma \approx 2.6$ can be extracted, which is slightly larger than that of $MoSe_2$ and MoS_2.[4,24,29] It is believed that further suppression of phonon scattering can be realized by employing the suitable substrate and the encapsulation of material in high-κ environment.[31]

Figure 3d unveils the dependence of conductance G on temperature under different V_{BG}. A metallic behavior typically occurs at high temperatures. The dashed line suggests that the temperature regime for the metallic behavior is enlarged when V_{BG} becomes larger, which is consistent with the previous studies on WS_2 and MoS_2.[29,32] Also, below 120 K the variation of G weakens for all V_{BG} values (Figure 3d). This can be attributed to the hopping of carriers through localized states which drives the system into a strongly localized regime as the hopping becomes dominant at lower temperatures.[33] As shown in Figure 3e, in the insulating regime (70–250 K), the temperature variation of G can be modeled with the thermally activated equation[34] $G(T) = G_0 \exp^{-E_a/k_BT}$, where E_a is the activation energy, k_B is the Boltzmann constant, and G_0 is a constant. The extracted E_a, which corresponds to the thermal activation of charge carriers at the Fermi energy into the conduction band, becomes smaller as the Fermi level moves toward the conduction band (Figure 3e, inset) in agreement with MoS_2 and WS_2 FET devices.[29,32] Moreover, at 20–250 K, the 2D variable range hopping model,[33,35] characterized by the equation $\sigma \propto \exp^{-(T_0/T)^{1/3}}$ provides an excellent description for the electrical transport of the ReS_2 nanosheets. The localization length can be determined using the equation $\zeta_{loc} = (13.8/k_BDT_0)^{1/2}$, where D is the density of states. Taking $D \approx 4 \times 10^{12}$ eV^{-1} cm^{-2} as the typical surface density of charge traps at the SiO_2 interface,[36,37] ξ_{loc} is estimated to be ≈5 nm at V_{BG} = 15 V, consistent with what attained in MoS_2 and WS_2.[32,33]

2.4. Performance of Few-Layer ReS_2-Based Photodetectors

Due to its sizeable direct bandgap of ≈1.5 eV, ReS_2 is anticipated to be a promising candidate for photodetection applications.[25,26] In view of this, two-terminal back-gate photodetectors based on few-layer ReS_2 were fabricated (see the Experimental

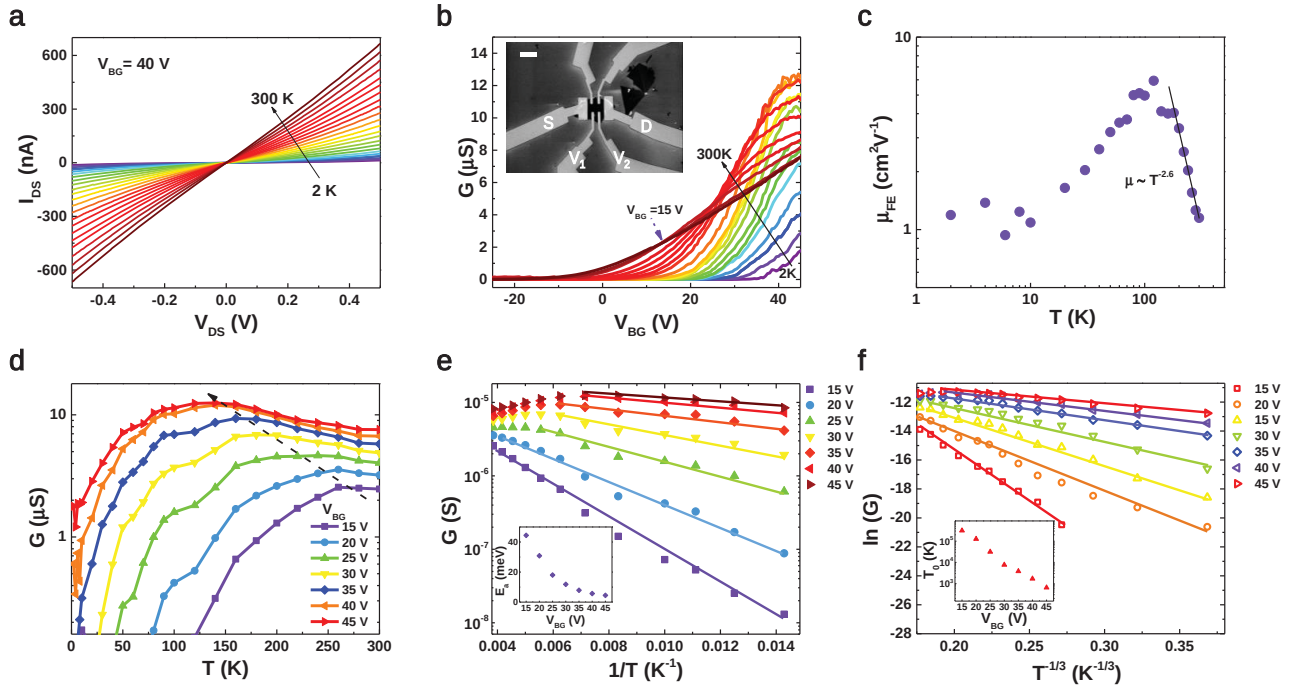

Figure 3. a) Double sweeps of I_{DS}–V_{DS} characteristics for several temperatures at fixed V_{BG} = 30 V with negligible hysteresis. b) Temperature dependence of the sheet conductivity on back-gate voltage. Inset shows the SEM image of the FET device. Scale bar, 5 μm. c) Extracted four-terminal field-effect mobility μ versus temperature T. The solid black lines are fits to the equation $\mu \propto T^{-\gamma}$ in the temperature range of 120–300 K. d) Sheet conductivity versus temperature at various back-gate voltages. e) Arrhenius plots of the sheet conductivity in the high-temperature range (70–250 K). Inset, the activation energy E_a as a function of back-gate voltage V_{BG}. f) Logarithm plots of sheet conductivity as a function of $T^{-1/3}$ for different back-gate voltages, from which the hopping parameter T_0 (inset) can be extracted (from the slopes of the line fits).

Section for details). As schematically depicted in **Figure 4**a, this type of device was probed using a focused laser beam (633 nm) and an illumination power ranging from 12.5 to 1000 nW. Figure 4b shows the quasilinear and symmetric I_{DS}–V_{DS} plots of the device with and without the laser illumination. Compared to the dark current background (black curve in Figure 4b), a significant increase of the photocurrent at a fixed V_{DS} bias was observed when the device was illuminated showing a strong dependence on the laser power. This can be explained by the increased number of photon-generated carriers. Time-resolved photoresponse behavior of the device was probed by switching the laser on and off. The device exhibits a stable and repeatable response to the laser illumination (Figure 4c). At V_{BG} = –10 V and V_{DS} = 50 mV, the device shows an on/off current of ≈56 and ≈20 nA, giving an on/off ratio of ≈2.8.

To further examine the photoresponse of the few-layer ReS_2 nanosheets, the I_{DS}–V_{DS} characteristics of the device under different illumination conditions were acquired. **Figure 5**a–h shows that the photocurrent I_{ph}, defined as $I_{ph} = I_{illuminated} - I_{dark}$ increases as V_{BG} increases. This is because the high V_{BG} can tune the Fermi level closer to the conduction band of ReS_2, which makes it easier for the tunneling and thermionic current

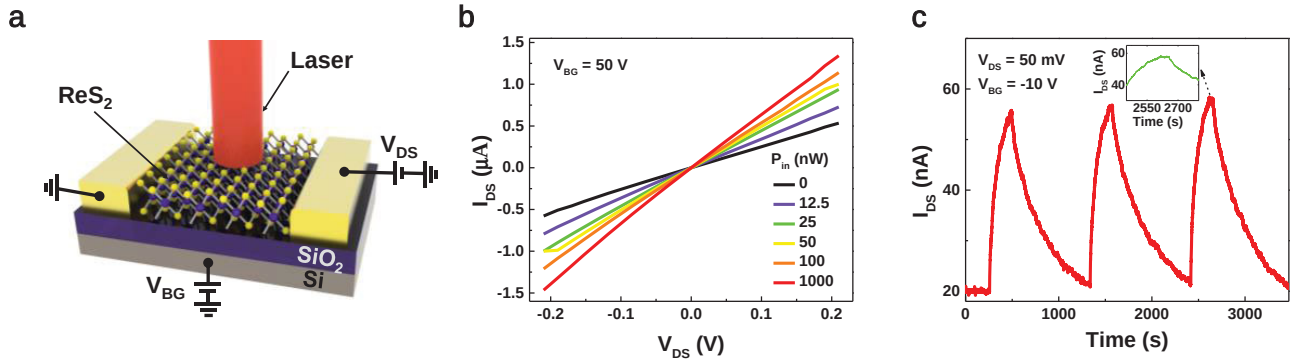

Figure 4. a) Schematic structure of ReS_2 back-gate photodetector. b) Output characteristics (I_{DS}–V_{DS}) of the device under different incident laser power P_{in}. c) Time-dependent I_{DS} of the device with and without the laser illumination. Inset, plot of the photoresponse peak over a small range, which shows a tendency toward saturation.

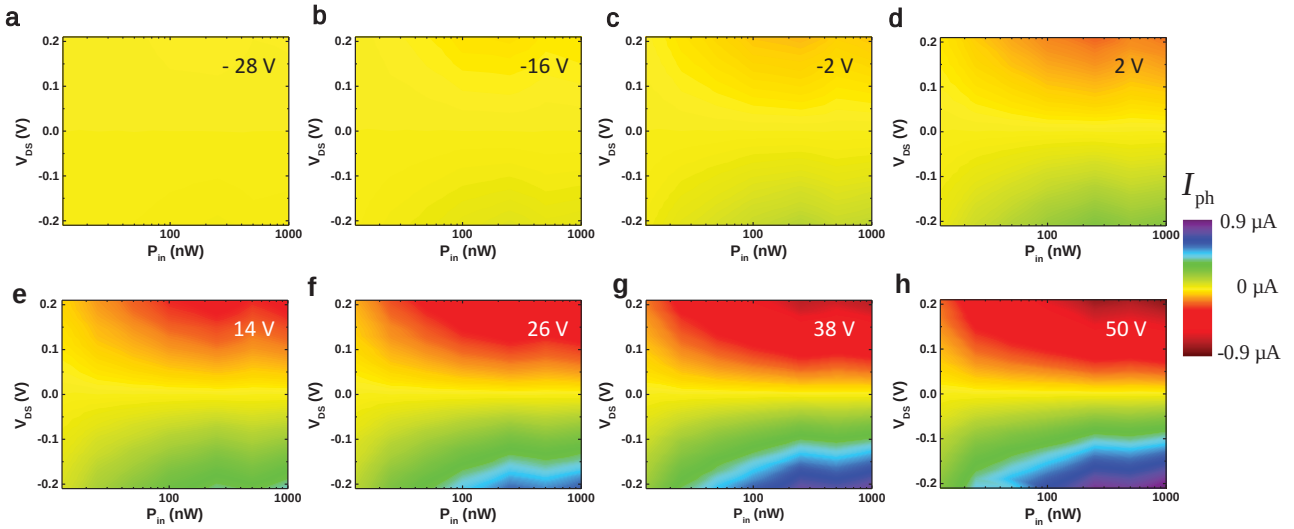

Figure 5. a–h) 2D mapping plots of I_{ph} as a function of V_{DS} and P_{in} acquired at different back-gate voltages. The highest I_{ph} corresponds to the largest V_{DS} of 50 V. The increase of V_{BG} gives rise to a higher I_{ph}, and a larger P_{in} at certain V_{BG} and also increases I_{ph}.

to overcome the barrier between the channel and electrodes. Moreover, the photocurrent I_{ph} also increases with the increase of V_{DS} owing to the enhancement of carrier drift-velocity and the reduction of the carrier transit time.[38]

External quantum efficiency (EQE) is an important parameter to reflect the ratio of electrons flowing out of the device in response to impinging photons,[23] and is defined as $EQE = I_{ph}/e\phi = (I_{ph}h\nu)/(qP_{in})$, where q is the electron charge, ϕ is the number of incident photon, h is the Planck constant, and ν is frequency of incident laser. The calculated EQE as a function of incident laser power and V_{BG} is presented in **Figure 6**a in a 2D map. The lower right corner exhibits the maximum value of EQE reaching 3168%, corresponding to a high back-gate voltage V_{BG} of 50 V and a low incident laser power P_{in} of 25 nW, thus showing a competitive device performance to those reported in InSe photodetectors.[23] At a fixed V_{BG} = 50 V (Figure 6b), the EQE reveals a linear decrease with increasing of the incident laser power. The trap states caused by defects or charge impurities in the ReS_2 channel and the adsorbents at ReS_2/SiO_2 interface account for such a decrease of EQE.[38,39] An increase in the laser power could reduce the generated carriers available for extraction owing to the creation of more traps being filled by photocarriers, leading to the saturation of the photocurrent and the dropping of EQE.[38–40] Photoresponsivity is another important parameter of the photodetectors,[41] defined as the ratio of the photocurrent to the incident laser power $R = I_{ph}/P_{in}$. Remarkably, the maximum value of the EQE corresponds to a photoresponsivity of 16.14 A W^{-1}, proving the ReS_2 to be a valuable material candidate for photodetection applications in addition to other 2D materials.[7,31,42,43]

3. Conclusion

We performed a comprehensive study of the electrical and optical properties of few-layer ReS_2 nanosheets. Top-gate FET devices exhibit an on/off current ratio over 10^6. Systematic temperature-dependent transport measurements reveal a metal-to-insulator transition in four-terminal devices. Few-layer ReS_2 photodetectors offer a good EQE of 3168% and

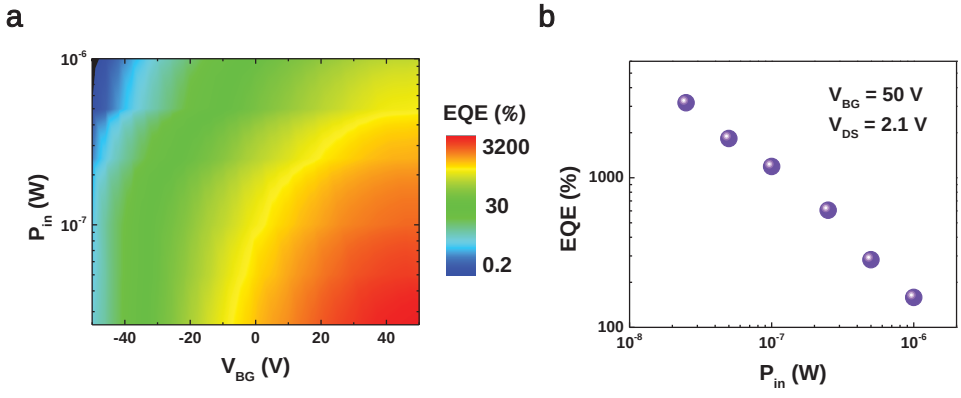

Figure 6. a) EQE as a function P_{in} and V_{BG} obtained at V_{DS} = 2.1 V. b) EQE as a function of P_{in} at fixed V_{BG} = 50 V, where EQE decreases as P_{in} increases due to the enhanced trap states. A high EQE value of 3168% is obtained when P_{in} = 25 nW.

high photoresponsivity of 16.14 A W^{-1}. Our results clearly identify the ReS_2 as a promising candidate for electronics and optoelectronics.

4. Experimental Section

Sample Growth: Few-layer ReS_2 nanosheets were synthesized in a horizontal tube furnace equipped with a 1 in. diameter quartz tube. SiO_2(285 nm)/Si substrates were loaded into the furnace and placed face-down above a crucible containing 1 mg of ReO_3 (≥99.9% Alfa Aesar). Another crucible containing 60 mg of sulfur (≥99.9% Alfa Aesar) was located upstream. The tube furnace was first pumped and flushed with argon gas in order to remove air. During the growth cycle, the tube furnace was maintained at 760 °C for 10 min. The argon gas was kept at a flow rate of 70 sccm at atmospheric pressure. The system was cooled down to room temperature naturally after the growth cycle was completed.

Top-Gate ReS_2 FET Device: The drain-source electrodes of the device were fabricated by EBL using PMMA/MMA bilayer polymer. Cr/Au (5 nm/80 nm) electrodes were deposited by e-beam evaporation. After lift-off, a 1 nm thick Al layer was deposited and oxidized in the air for 24 h, acting as a seed layer for subsequent deposition of an Al_2O_3 (30 nm) dielectric layer via ALD. During the ALD process, trimethylaluminum reacted with water to produce Al_2O_3 at 200 °C in a vacuum chamber. Another EBL and metal deposition process was used for the top-gate (Cr/Au 5 nm/80 nm) electrode fabrication, after which the device was annealed for 2 h at 200 °C in an argon atmosphere. Room temperature electrical properties of the devices were measured in a probe station using a semiconductor device parameter analyzer (Agilent, B1500A).

ReS_2 Back-Gate Device for Low Temperature and Optical Measurements: An EBL and metal deposition process was used in the device fabrication. The temperature-dependent transport measurements of the four-terminal device were carried out in a physical property measurement system (PPMS) (quantum design) using an Agilent 2912. A focused laser with a wavelength of 633 nm was used for measurements of optical properties of the devices. A 2 h annealing step at 200 °C in an argon atmosphere of the device was also taken before the measurement.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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